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EXAMINER

KESHAVAN, BELUR V

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/036,020

Applicant(s)

CHITTIPEDDI ET AL.

Examiner

Belur V Keshavan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 15-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3,5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-14 are drawn to an integrated circuit structure , classified in class 257, subclass 369.
- II. Claims 15-24 are drawn to a method for fabricating an integrated circuit structure, classified in class 438, subclass 199.

The inventions are distinct, each from the other because of the following reasons:

Inventions of Group I and Group II are related as a product made and a process of making the product. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case inventions of Group I can be made by ROX isolation between the first and the second device regions instead of electrical insulator filled trench isolation as claimed in claim 15.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. John L. DeAngelis, Jr., on 07/25/03 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-14. Affirmation of this election must be made by applicant in replying to this Office action. Claims

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15-24 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

The drawings are objected to because the following informalities.

In figures 3-8, P- and P+ must be interchanged for consistency with the figures 9-39 and to commensurate with description given in the specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

In figure 7, P- is shown as 106 instead of 100. Appropriate correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. In claim 11, the feature "a third conductive element electrically connecting the first and the second source/drain regions" is not shown. Therefore, this feature must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Abstract

Applicant is reminded format for an abstract of the disclosure. The abstract should be in narrative and generally limited to a single paragraph. The abstract is in two paragraphs and appropriate correction is required to reduce the abstract to a single paragraph.

Specification

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with errors. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some of the errors in the specification are:

On page 9, line 16, "p-doped" must be n-doped.

On page 10, line 19, "p-channel" must be n-channel.

On page 10, line 20, "n-channel" must be p-channel.

The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph with out adding new matter.

Claim Objection

Claim 2 is objected under 37CFR 1.75 D, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 2 and line 4, the word "third doped" is confusing. The examiner suggests using ---second doped--- instead.

Any further rejections of, or indications of allowability of claim 2 and its dependent claim 3 are based on claims 2 and 3 as they are understood by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Layman et al.

(Pub. No.: US 2003/0060015 A1) hereinafter Layman.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1-6 Layman teaches, in figures 5, 7, 11, 13 and 14, an integrated circuit structure wherein the first (210A) and the second (212A) MOSFETs form a complimentary MOSFET pair of transistors and comprising:

A semiconductor layer (100) having a major surface (106) formed along a plane; a first (116) and a second (118) spaced-apart doped region formed in the surface; an isolation region (108) disposed between the first and the second regions for electrically insulating the first and the second regions, the electrically insulating material being silicon dioxide (110); a plurality of

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layers (120, 122, 124, 126, 130, 134, 136, 138) overlying the first doped region including a first (142) and a second (144) trench therein where the first doped region is a first source/drain region of a first MOSFET (210A) and the second doped region is a first source/drain region of a second MOSFET (212A); a third doped region (160) formed in the first trench over the first doped region and of a different conductivity type than the first doped region wherein the third doped region forms the channel region of the first MOSFET; a fourth doped region (162) formed in the second trench over the second doped region and of a different conductivity type than the second doped region wherein the fourth doped region forms the channel region of the second MOSFET; a first oxide layer (220A) proximate to the third doped region; and a second oxide layer (222A) proximate the fourth doped region.

Regarding claim 7, Lyman teaches, in figure 13, of removing one of the plurality of layers (130) to expose a portion over the third doped region in the first trench and a portion of the fourth doped region in the second trench and wherein the first oxide layer is proximate the exposed portion of the third doped region and wherein the second oxide layer is proximate the exposed portion of the fourth doped region.

Regarding claim 8, Lyman teaches, in figure 13, the following: a fifth doped region (153) overlying the first doped region and of the same conductivity type as the first doped region, wherein the first doped region is a first source/drain region of the first MOSFET and wherein the fifth doped region is a second source/drain region of the first MOSFET and wherein the third doped region is a channel region of the first MOSFET; a sixth doped region (154) overlying the second doped region of the same conductivity type as the second doped region wherein the second doped region is a first source/drain region of the second MOSFET; wherein the sixth

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doped region is a second source/drain region of the second MOSFET; wherein the fourth doped region is a channel region of the second MOSFET; wherein the first oxide layer is a gate oxide layer of the first MOSFET and; wherein the second oxide layer is a gate oxide layer of the second MOSFET.

Regarding claims 9 and 10, Lyman teaches in paragraph [0043] and in figure 17, a first (230) and a second (234) conductive elements comprising polysilicon adjacent to the first and second gate oxide layers to control the operation of the first and second MOSFETs as their respective gate.

Regarding claim 11, Lyman teaches further in figure 13, a third conductive element (164, 166) electrically connecting the first and the second source/drain regions.

Regarding claim 12, Lyman teaches in paragraph [0042] and in figure 11, that layers 126 and 134 are doped insulating layers in the plurality of layers and serving as a dopant source to diffuse dopants into the third and the fourth doped regions.

Regarding claim 13, Lyman teaches in paragraph [0042] that the third and fourth doped regions each form a channel region and wherein the dopants diffused from the doped insulating region form source/drain extensions within each of the channel regions.

Regarding claim 14, Lyman teaches in figures 5, 7, 11, 13 and 14 an integrated circuit structure comprising: a semiconductor layer (100) having a major surface (106) formed along a plane; a first (116) and a second (118) doped source/drain region formed in the major surface; an isolation region (108) disposed between the first and the second source/drain regions for electrically insulating the first and the second source/drain regions; a plurality of layers (120, 122, 124, 126, 130, 134, 136 and 138) overlying the first and the second source/drain regions

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including a first (142) and a second (144) trench formed therein; a first doped channel region (160) formed in the first trench overlying the first source/drain region and having a different conductivity type than the first source/drain region (please see paragraph [0037]); a second doped channel region formed in the second trench overlying the second source/drain region and having a different conductivity type than the second source/drain region (please see paragraph [0037]); a third (153) and a fourth (154) doped spaced apart source/drain region wherein the third source/drain region is vertically aligned with the first channel region (160) and the first source/drain region, and wherein the fourth source/drain region is vertically aligned with the second source/drain region (162) and the second channel region, and wherein the third source/drain region is of the same conductivity type as the first source/drain region, and wherein the fourth source/drain region is of the same conductivity type as the second source/drain region; a first oxide layer (220A) proximate to the first channel region and a second oxide layer (222A) proximate the second channel region.


Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 703 306 5985. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703 308 1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703- 872-9318 for regular communications and 703-872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

Bvk 
August 4, 2003.

Belur V. Keshavan
Examiner, Art Unit.



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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